

**WHAT IS CLAIMED IS:**

1. A thin film transistor array panel comprising:
  - an insulating substrate;
  - a gate wire formed on the insulating substrate and including a plurality of
  - 5 gate lines, a plurality of gate electrodes, and a plurality of gate pads connected to one ends of the gate lines;
  - a storage electrode wire formed on the insulating substrate and including a plurality of storage electrode lines and a plurality of storage electrodes;
  - a gate insulating layer formed on the gate wire and the storage electrode
  - 10 wire;
  - a semiconductor layer formed on the gate insulating layer;
  - a data wire formed on the gate insulating layer and including a plurality of data lines insulated from and crossing over the gate lines, a plurality of source electrodes contacting the semiconductor layer in part, a plurality of drain electrodes
  - 15 facing the source electrodes and contacting the semiconductor layer in part, and a plurality of data pads connected to one ends of the data lines;
  - a passivation layer formed on the data wire;
  - a plurality of pixel electrodes formed on the passivation layer and electrically connected to the drain electrodes; and
  - 20 a plurality of storage electrode connections formed on the passivation layer and connecting the storage electrode lines and the storage electrodes facing across the gate lines.
2. A thin film transistor array panel comprising:
  - an insulating substrate;
  - 25 a gate wire formed on the insulating substrate and including a plurality of gate lines, a plurality of gate electrodes, and a plurality of gate pads connected to one ends of the gate lines;
  - a storage electrode wire formed on the insulating substrate and including a plurality of storage electrode lines and a plurality of storage electrodes;
  - 30 a gate insulating layer formed on the gate wire;
  - a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and having a triple-layered structure including an amorphous silicon layer, an ohmic contact layer, and a metal layer, the data wire including a plurality of data lines, a plurality of source electrodes connected to the data lines, a plurality of drain electrodes facing the  
5 source electrodes, and a plurality of data pads;

a passivation layer formed on the data wire;

a plurality of pixel electrodes formed on the passivation layer and electrically connected to the drain electrodes; and

a plurality of storage electrode connections formed on the passivation  
10 layer and connecting the storage electrode lines and the storage electrodes facing across the gate lines.

3. The thin film transistor array panel of claim 1 or 2, further comprising a plurality of color filters disposed between the data wire and the passivation layer.

15 4. The thin film transistor array panel of claim 1 or 2, further comprising a common bar connected to one ends of all the storage electrode lines.

5. A thin film transistor array panel comprising:

an insulating substrate;

a first signal line formed on the insulating substrate and extending in a  
20 transverse direction;

a second signal line formed on the insulating substrate and extending in a transverse direction;

a third signal line insulated from and crossing over the first and second and extending in a longitudinal direction;

25 a plurality of pixel electrodes in pixel areas defined by intersections of the first signal lines and the third signal lines; and

a plurality of thin film transistors connected to the first signal lines, the third signal lines, and the pixel electrodes,

wherein the second signal lines are connected to each other via connecting  
30 paths provided on the pixel areas.

6. The thin film transistor array panel of claim 5, further comprising a common bar connecting one ends of the second signal lines.

7. A thin film transistor array panel comprising:  
an insulating substrate;

5 a plurality of first signal lines formed on the insulating substrate, extending in a transverse direction, and including a plurality of first signal pads;

a plurality of second signal lines formed on the insulating substrate and extending in a transverse direction;

10 a plurality of third signal lines insulated from and intersecting the first and the second signal lines, extending in a longitudinal direction, and including a plurality of third signal pads;

a plurality of pixel electrodes provided on pixel areas defined by intersections of the first signal lines and the third signal lines;

15 a plurality of signal lines connected to the first signal lines, the third signal lines, and the pixel electrodes;

a first common bar connecting ends of the second signal lines located opposite the first signal pads; and

a second common bar connecting ends of the second signal lines located near the first signal pads,

20 wherein the second the common bar has a width equal to or less than 150 microns.